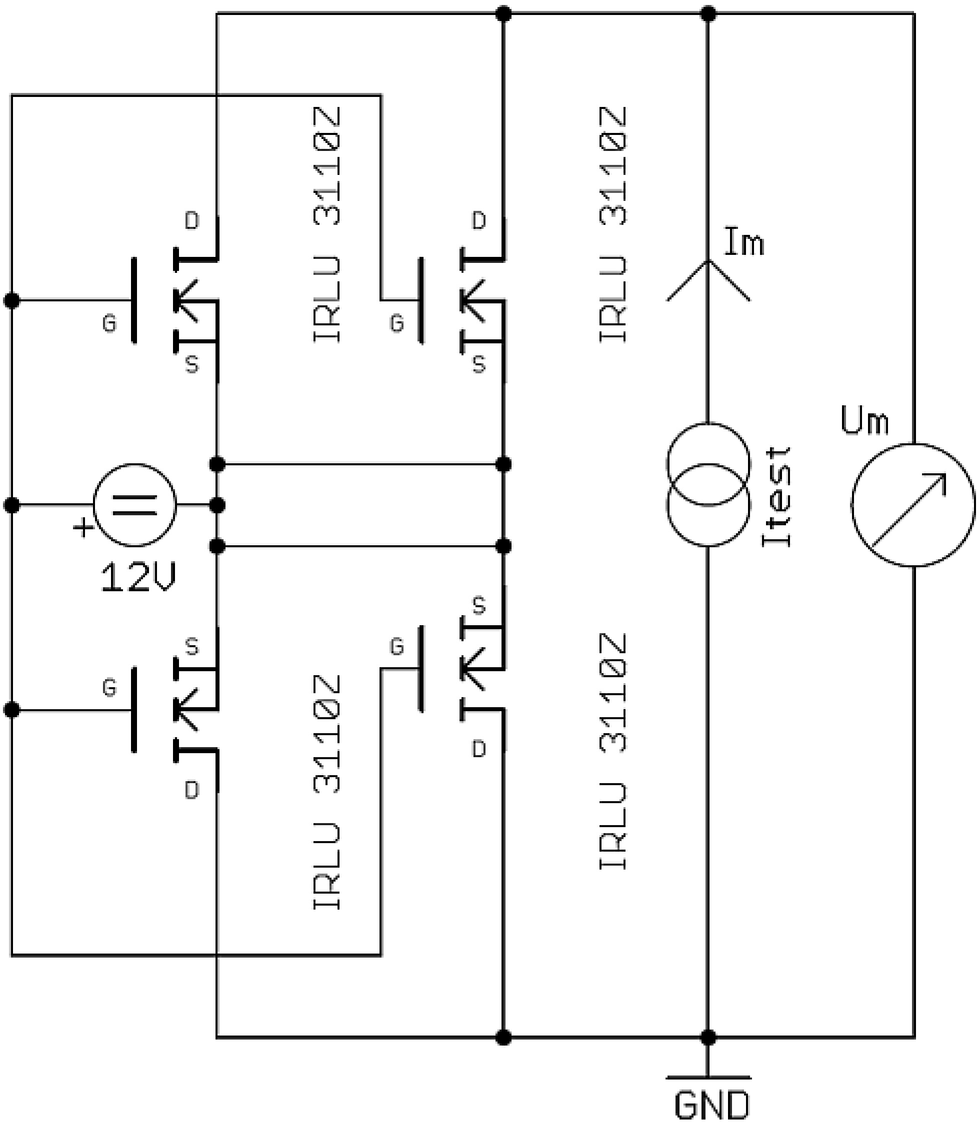
Appendix A

SSR and THD

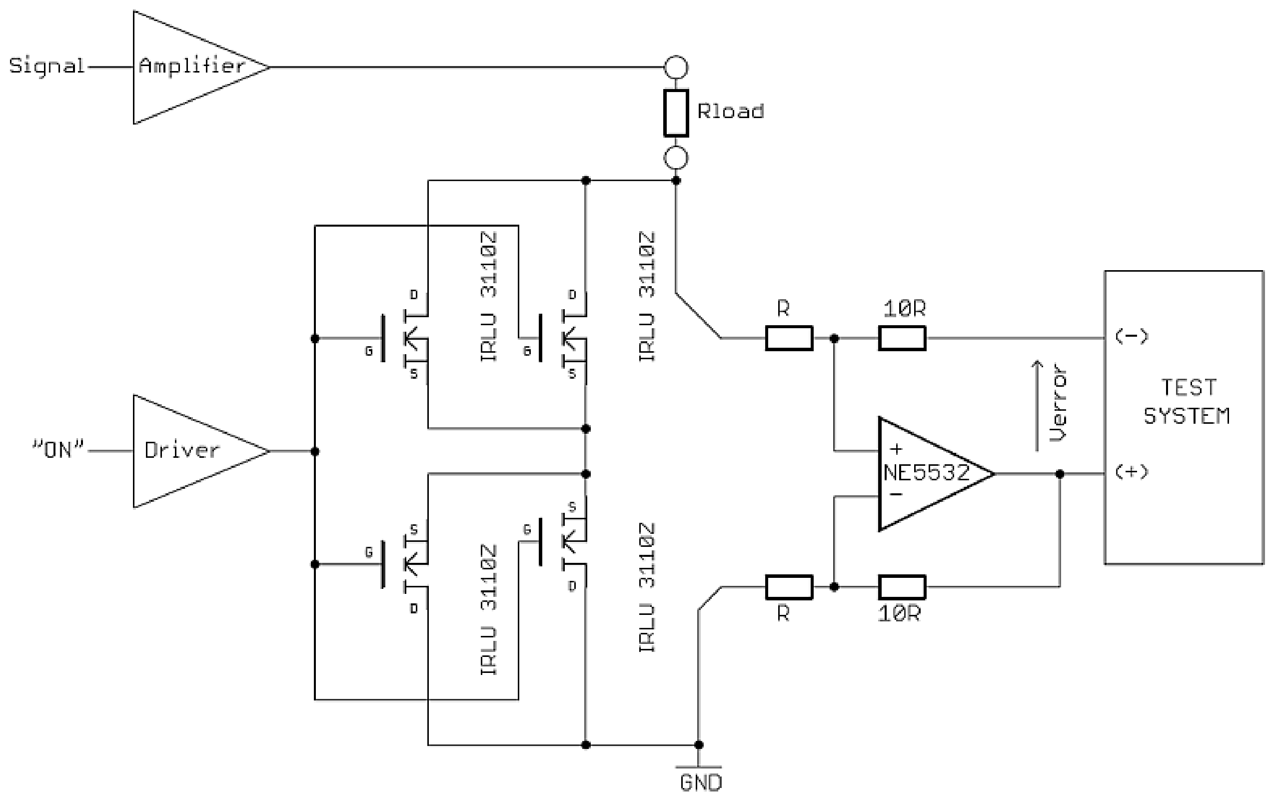
The first thought when hearing SSR is, that it creates THD. But why ? There are no measurements around, but he feeling it creates THD is widely spreaded, especially in audiophile circles.

So making a simulation as first step is a good idea. Fortunately, for the choosen FETs simulation models are available from International Rectifier, wich normally give good results regarding the real devices. So, have a look on fig.1 to see the simulation shematic:



Now, you can run a DC Transfer Analysis with Itest as parameter (0.01A .. 10A).
Then, knowing that R=U/I, you can plot R=Um/Im and see a very slow ascending line. This is the Rdson over current. After zooming in you see that Rdson will raise with ~1.35µOhm / 10A. Having 11mOhm as constant Rdson and 135nOhm per A, the ratio will be ~ 80.000. If using 4 Ohms as usual load, the factor 4 Ohms/10mOhms will be 400. The total ratio of Rl to nonlinearity will be 80.000 x 400 = 32 million (per Ampere) and this is somewhere in the 150 dB range. Now using not 1A but 10A as peak current, THD will be in the >130 dB range. From simulation, the amplifier would be always worse than the SSR.
Measuring total SSR drop volatge Um and current Im when running 10Apk and then building Rdson gives a deltaRdson of 0.64µohms resultung in 125dB.

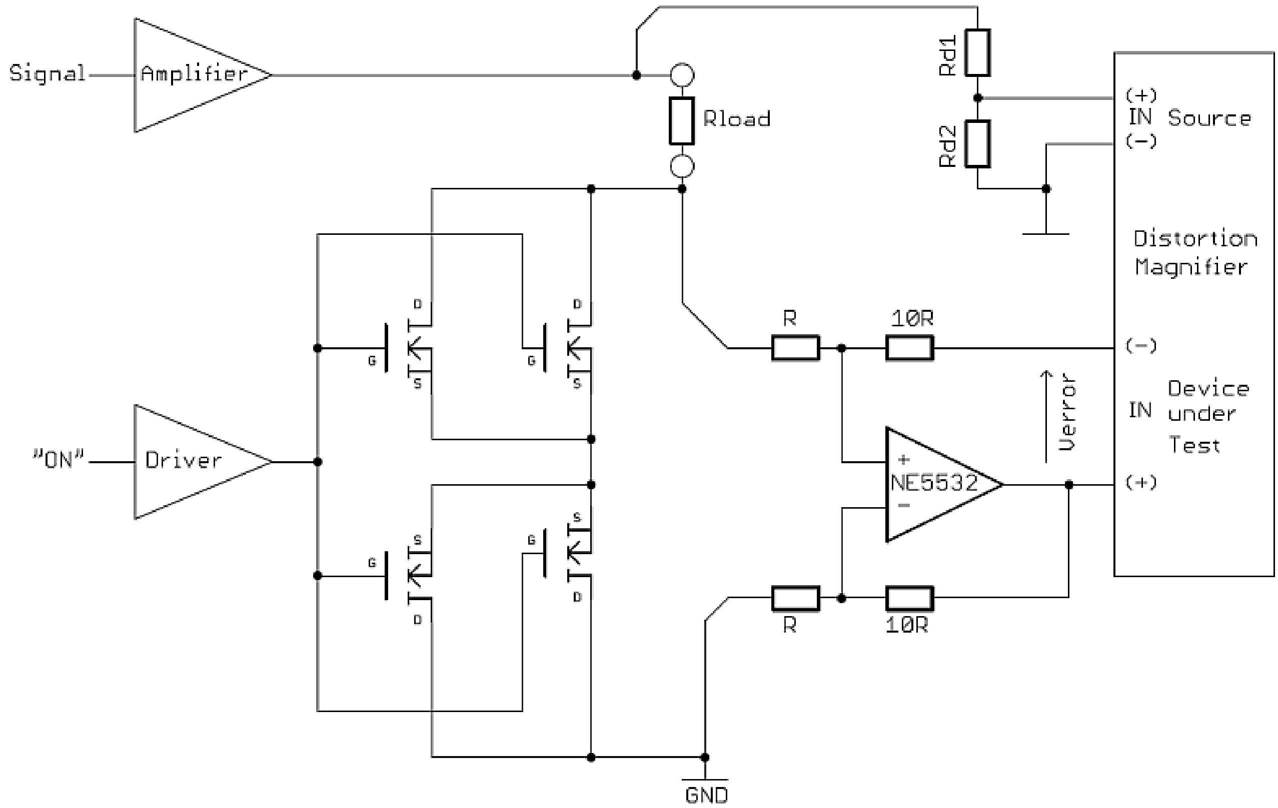
Going to the real world, the THD can be measured best with an real amplifier, because of the high currents necessary. See fig.2 for measurement arrangement:



The test setup consist of an amplifer capable of several amperes output current, a load resistance in the range usually used , like 4 or 8 ohms, the SSR driver, a differential preamplifier with gain=10 and a test system to measure the THD figure. The test system can be something like a preofessional one, a distortion magnifier or a good soundcard. Now, a sine signal schould be inserted with a level so that, at the load, a usefull current flow is establisched (e.g. 5A..7A peak). Then the voltage drop over the SSR is measured and amplified by 10. With the FET's given and 7.5A peak, my test setup gives a voltage drop of ~ 100mV peak wich results in ~1Vpeak level at the analyzer input. Measuring the THD now, you see the two things, the THD the amplifier makes and the THD resulting from the SSR. With normal test equipment, you can only measure both and if you compare it with the amplifier THD, you can see if it get's worse or not.

Going deeper

Going deeper is possible, but you need a distortion magnifier with the source input connected to the downscaled amplifier output and the DUT input connected to the differential amplifiers output. Then, the magnifier substract it's source input from the signal related part of the voltage over the SSR and remaining is the SSRs THD only. The THD could now be magnified by 10 or 100.



The THD of the SSR can now be calulated as

THD = (Gda / Gdm) * (Rdson/Rload) * (Distortion magnifier output)

with

Gdm	Gain of ditortion magnifier (x1, x10, x100 typical)
Gda	Gain of differential Amplifier (x10 in with values given)
Rload	Load resistance in ohms
Rdson	Static Rdson of SSR = ~ (Verror / Gda) / (Voutpk / Rload) if Rdson << Rload
10R;R	10R = 10x value of R, R=100; 10R=1k is usefull

typical values: Gdm =100; Gda=10; Rload=4ohms; Rdson= 10mohms
THD = (10/100)*(10m/4)*Output = 250E-6*Output

The THD of the NE5532 can be ignored, because you will get a voltage in the 100mV range multiplied by ten giving ~1 V. If the NE5532 would have a THD of -90dB only, than the SSRs THD is by the factor Rload/ Rdson better than measured (regarding the formula given above). With this factor of 400 (e.g.) , you would get another 50dB and end up in the 140dB range. That's low enough, even for the best amplifiers.

Note: You must calculate the Rd1/Rd2 divider so that at the measurement voltage ~1Vpk is measured at the Source input. With a slightly modified Distortion magnifier (gain is -3dB..+3dB) the test should work.

Other effects

We have seen that the THD of a SSR is only dependent on it's Rdson variation. The first parameter, Current, we have examined earlier. But there are others and one additional nonlinearity, if not the 2nd major one, is tepmerature. The nonlinearity wouldn't matter, if temperature rise is slowly, e.g. 1°C/sec. But if it rises very fast, you would modulate the Rdson by temperature wich is signal dependent !

The Rdson vs. Temp. graph in the IRLR3110 datasheet shows us, that for a 0...100°C change the Rdson varies from 0.75*Rdson to 1.75*Rdson (relative to 25°C). Approximating it with a line and 14mR, we get 10.5mR to 24.5mR for 100°C change, giving 140µohms per °C. Now, how warm would the die be ? Using 2 paralleled devices, like done here, everyone get's half the current. This is 5A/device if max is 10A. Power dissapation is now I*I*R=5A*5A*14mR=350mWpeak and 3.5A*3.5A*14mR=175mWrms per device. Worst thing what can happen are low frequency pulses, because of at high frequencies (e.g. > 1kHz), the die wouldn't heat up and cool down fast enough.

The internal thermal resistance is 1.05K/W, so giving ~ +0.37°C at 350mW and 0.184K at 175mW. These values related with the 140µohms/K give a thermal nonlinearity of 52µohmspk or 26µohms rms. Our 4Ohms load divided by 52µohms will give ~ 98dB THD, the 26µohms rms will give ~ 103dB. This effect covers the effect of current dependent Rdson completely ! But fortunately, Audio wouldn't consist of power peaks only. Lowering the volume by 6dB will give 15Vpk only, wich pushes 3.75Apk through the load, so a single device sees 1.88A wich results in 1.88A*1.88A*14mR =50mWpeak, wichare mutliplied by 1.05, giving 52mK of temperature rise and therefore 7.3µohms. In the end, the ratio is ~115dB and getting even lower with decreasing output voltage.

Also here, a simulation was done with the following results:

10.49mohms @ 0°C and 11.05mohms @ 100°C with 1A current giving 115µohms per 100°C and 1.15µohms per 1°C. Let it run with 10Apeak give an Ppeak of 270mW per device wich would result in 0.28°C temperature swing per device. Total Rdson change is therefore 1.15µohms*0.28°C = 322nohms. The ratio Rload and deltaRdson is then 142dB. So simulation gives better results than datasheet and assumptions do.

Also take into account, that we assumed that there is almost no thermal mass of the device, averaging the temperature rise and cool down, so the values given here are the worst case , and values are better in reality. Using a more realistic 20°C to 80°C range (60°C), then you get 14mR..21mR, resulting in 120µohms. This is a factor, giving another 1.4dB and for very small temperature changes around the 20°C-40°C, the value is even lower.

But for higher currents than these 5A per device, other FETs or more paralleled ones should be choosen.

The third, but mainly neglible, effect is Vgs, the gate to source voltage. Rdson is dependent of Vgs. But usually, it shouldn't be a problem to hold Vgs constant and Vgs should be in a range, where it's value has almost no influence on Rdson. If you go up to 12V and higher, the dependencies are very low.

Small Signal SSR:

For interest I have added some information of small signal FETs. But take care of the output capacity if the FET is set to OFF.

All values simulated with SSR in GND line, so switching R=1k to GND ("Lowside").
VgsON=12V;VgsOFF=0V

Simulation results:

FET	Rdson static [Ohms]	delta Rdson 1nA .. 2mA [Ohms]	Voltage at SSR [V/mA]	OFF leakage at 1V/1kohm	Ratio delta Rdson to 1kohm	THD 2V/1kohm [dB]
BSS138	2,25	5,1 µohms	2,25m	762pA	1,96E+008	> 160
BSS138, PI*	4,5	15 µohms/0.5mA	4,5m		6,60E+007	155
BS170	4,4	40 nohms	4,4m	5,6pA	2,50E+010	> 160
BSS123	5,2	10 µohms	5,2m	33pA	> 1,0E+008	> 160
IRLML0030	0,04	240 nohms	35µ	8,12nA	1,00E+014	> 180

*IRLML0030:
Datasheet -> deltaRdson=3mR/25A = 240nohm
Cout ~ 100pF --> 1kOhms:-3dB @ 800kHz (OFF)
cost ~ 0,20€/piece, Jan 2015

FETs simulated from Signal Source to R=1k ("Highside"):

FET	Rdson static [Ohms]	delta Rdson 1nA .. 2mA [Ohms]	Voltage at SSR [V/mA]	OFF leakage at 1V/1kohm	Ratio delta Rdson to 1kohm	THD 2V/1kohm [dB]
BSS138, PI*	4,5	15 µohms/0.5mA	4,5m	1E-17 A	6,60E+007	155

FET	Loss @ 22kHz* (OFF)	Loss @ 100kHz* (OFF)	Loss @ 1 Mhz* (OFF)
IRLML0030	-36 dB	-22 dB	-4,5 dB
BSS138	-58 dB	-45 dB	-25 dB

*Loss means by what factor the original source signal is supressed by the turned OFF FET
*PI configuration: